EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	25324338	@ad<"20040211"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/08/22 18:23
L2	9482	(plurality or multiple) adj2 bank$2	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/08/22 19:25
L3	8296	first adj2 bank$2	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/08/22 19:25
L4	7351	second adj2 bank$2	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/08/22 19:26
L5	392	size near3 ("same" or equal$4) near5 bank$2	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/08/22 19:27
L6	10694	first adj2 adder	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/08/22 19:27
L7	12145	second adj2 adder	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/08/22 19:31
L8	467	second adj row adj address	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/08/22 19:28
L9	847	first adj row adj address	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/08/22 19:28

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L10	8304	6 and 7	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/08/22 19:28
L11	386	8 and 9	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/08/22 19:28
L12	1557	2 and 3 and 4	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/08/22 19:29
L13	50	12 and 5	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/08/22 19:29
L14	0	10 and 13	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/08/22 19:30
L15	2	11 and 13	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/08/22 19:30
L16	175243	adder or (add$5 adj unit$2)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/08/22 19:31
L17	5	13 and 16	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/08/22 19:32
L18	4	1 and 17	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/08/22 19:32
L19	2	1 and 15	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/08/22 19:32

EAST Search History

L20	6	18 or 19	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/08/22 19:32

Terms used
memory bank interleav simultaneous unaligned adder memory row address

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1 A survey of commercial parallel processors

Edward Gehringer, Janne Abullarade, Michael H. Gulyn

September 1988 **ACM SIGARCH Computer Architecture News**, Volume 16 Issue 4

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Full text available: pdf(2.96 MB) Additional Information: full citation, abstract, citings, index terms

This paper compares eight commercial parallel processors along several dimensions. The processors include four shared-bus multiprocessors (the Encore Multimax, the Sequent Balance system, the Alliant FX series, and the ELXSI System 6400) and four network multiprocessors (the BBN Butterfly, the NCUBE, the Intel iPSC/2, and the FPS T Series). The paper contrasts the computers from the standpoint of interconnection structures, memory configurations, and interprocessor communication. Also, the share ...

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A survey of commercial parallel processors

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Authors Edward Gehringer Computer Systems Laboratory, North Carolina State University, Raleigh, NC
Janne Abullarade Computer Systems Laboratory, North Carolina State University, Raleigh, NC
Michael H. Gulyn Computer Systems Laboratory, North Carolina State University, Raleigh, NC

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↑ ABSTRACT

This paper compares eight commercial parallel processors along several dimensions. The processors include four shared-bus multiprocessors (the Encore Multimax, the Sequent Balance system, the Alliant FX series, and the ELXSI System 6400) and four network multiprocessors (the BBN Butterfly, the NCUBE, the Intel iPSC/2, and the FPS T Series). The paper contrasts the computers from the standpoint of interconnection structures, memory configurations, and interprocessor communication. Also, the shared-bus multiprocessors are compared in terms of cache-coherence strategies, and the network multiprocessors are compared in terms of node structure. Where possible, price and performance information has been included. The reader is cautioned that this survey is based largely on information submitted by manufacturers; the authors have not performed any independent evaluation.

↑ CITINGS

G. J. Murakami , R. H. Campbell , M. Faiman, Pulsa: non-blocking packet switching with shift-register rings, ACM SIGCOMM Computer Communication Review, v.20 n.4, p.145-155, Sep. 1990

↑ INDEX TERMS

Primary Classification:
C. Computer Systems Organization

↳ **C.1** PROCESSOR ARCHITECTURES
↳ **C.1.2** Multiple Data Stream Architectures (Multiprocessors)
↳ **Subjects:** Parallel processors**

Additional Classification:
C. Computer Systems Organization
↳ **C.1** PROCESSOR ARCHITECTURES
↳ **C.1.2** Multiple Data Stream Architectures (Multiprocessors)
↳ **Subjects:** Interconnection architectures (e.g., common bus, multiport memory, crossbar switch)

K. Computing Milieux
↳ **K.1** THE COMPUTER INDUSTRY
↳ **Subjects:** Suppliers; Statistics

General Terms:
Design, Measurement, Performance

↑ **Collaborative Colleagues:**

Janne Abullarade:	Edward Gehringer
	Michael H. Gulyn
Edward Gehringer:	Janne Abullarade
	Prashant Baheti
	Michael H. Gulyn
	Chih-Wei Ho
	Nachiappan Nagappan
	Somik Raha
	David Stotts
	Laurie Williams
Michael H. Gulyn:	Janne Abullarade
	Edward Gehringer

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#7	(data aligner<IN>metadata)
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